SN74LV1T125 Single Power Supply Single Buffer Gate with 3-State Output CMOS Logic Level Shifter

1 Features

- Single-Supply Voltage Translator at 5.0/3.3/2.5/1.8V V_{CC}
- Operating Range of 1.8V to 5.5V
- Up Translation
  - 1.2V(1) to 1.8V at 1.8V V_{CC}
  - 1.5V(1) to 2.5V at 2.5V V_{CC}
  - 1.8V(1) to 3.3V at 3.3V V_{CC}
  - 3.3V to 5.0V at 5.0VV_{CC}
- Down Translation
  - 3.3V to 1.8V at 1.8V V_{CC}
  - 3.3V to 2.5V at 2.5V V_{CC}
  - 5.0V to 3.3V at 3.3V V_{CC}
- Logic Output is Referenced to V_{CC}
- Output Drive
  - 8.0mA Output Drive at 5.0V
  - 7.0mA Output Drive at 3.3V
  - 3.0mA Output Drive at 1.8V
- Characterized up to 50MHz at 3.3V V_{CC}
- 5.0V Tolerance on Input Pins
- –40°C to 125°C Operating Temperature Range
- Latch-Up Performance Exceeds 250mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Supports Standard Logic Pinouts
- CMOS Output B Compatible with AUP1G and LVC1G Families

(1) Refer to the V_{IH}/V_{IL} and output drive for lower V_{CC} condition

2 Applications

- Industrial controllers
- Telecom
- Portable applications
- Servers
- PC and notebooks
- Automotive

3 Description

SN74LV1T125 is a low voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, telecom, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8V/2.5V/3.3V/5V CMOS levels.

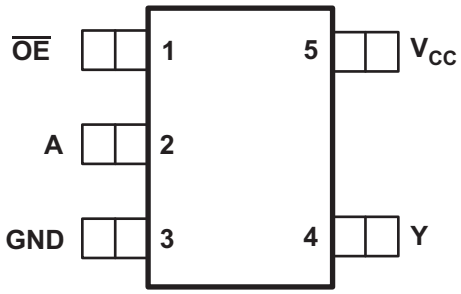
The input is designed with a lower threshold circuit to match 1.8V input logic at V_{CC} = 3.3V and can be used in 1.8V to 3.3V level up translation. In addition, the 5V tolerant input pins enable down translation (e.g. 3.3V to 2.5V output at V_{CC} = 2.5V). The wide V_{CC} range of 1.8V to 5.5V allows generation of desired output levels to connect to controllers or processors.

The SN74LV1T125 is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SN74LV1T125DBVR	SOT-23 (5)	2,90mm x 1,60mm
SN74LV1T125DCKR	SC70 (5)	2,00mm x 1,25mm

DCK or DBV PACKAGE
(TOP VIEW)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2013) to Revision A	Page
• Updated document formatting.	1

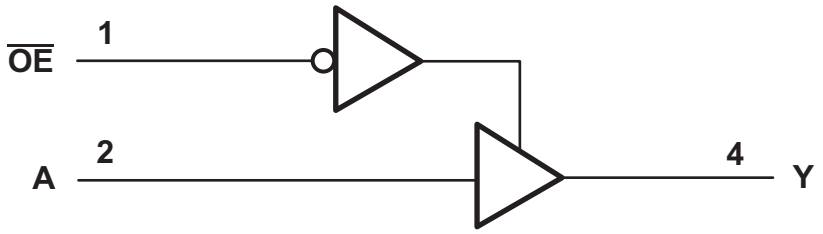
Function Table

INPUT (Lower Level Input)		OUTPUT (V_{CC} CMOS)
OE (1)	A	Y
L	H	H
L	L	L
H	X	Z

(1) Not recommend to floating OE pin for signal oscillation

SUPPLY Vcc = 3.3V		
INPUT (Lower Level Input)		OUTPUT (V_{CC} CMOS)
A	B	Y
VIH(min) =1.35 V VIL(max) =0.8 V		VOH(min) = 2.9 V VOL(max)= 0.2 V

4.1 Logic Diagram



Switching Characteristics at 50 MHz

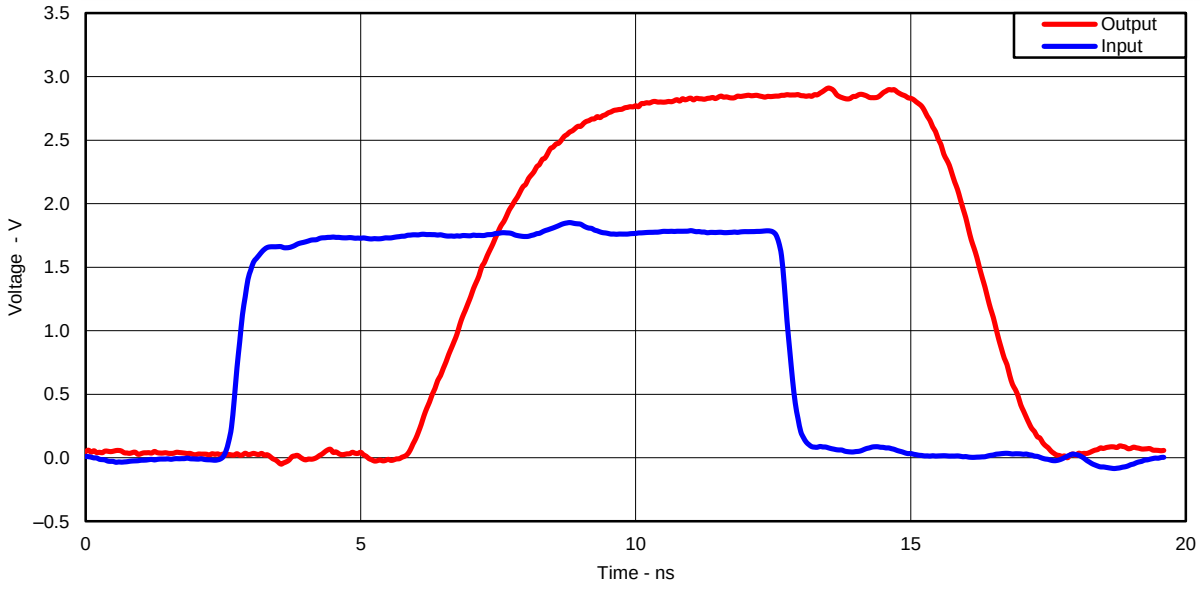


Figure 1. Excellent Signal Integrity (1.8V to 3.3V at 3.3V V_{CC})

Logic Diagram (continued)

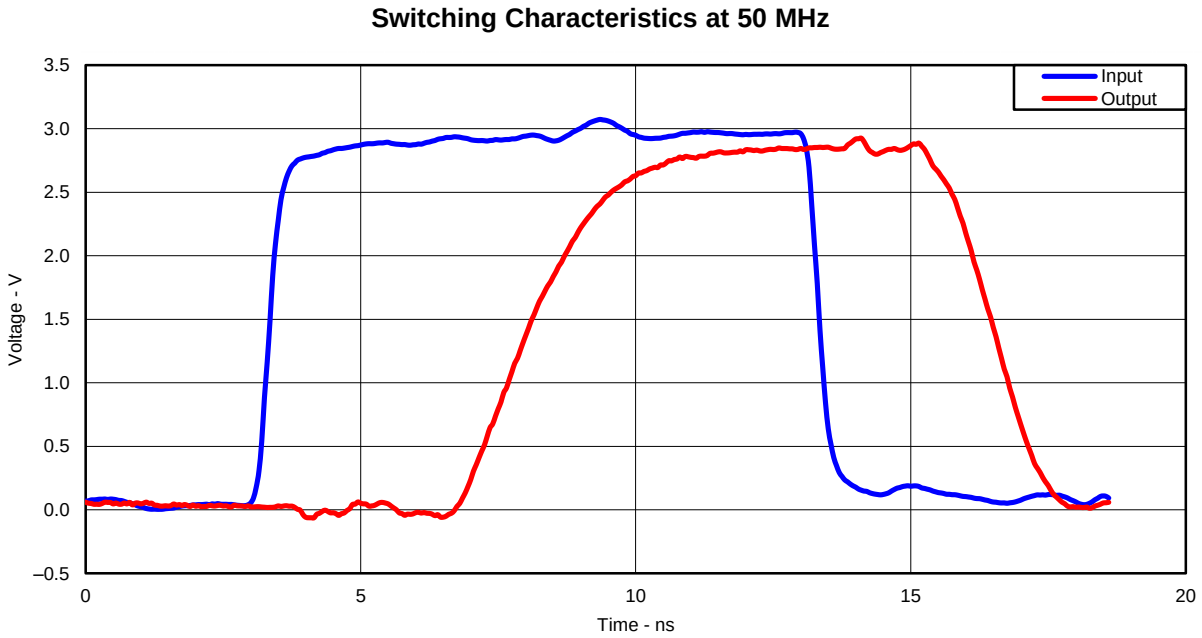


Figure 2. Excellent Signal Integrity (3.3V to 3.3V at 3.3V V_{CC})

Figure 3. Switching Characteristics at 15 MHz

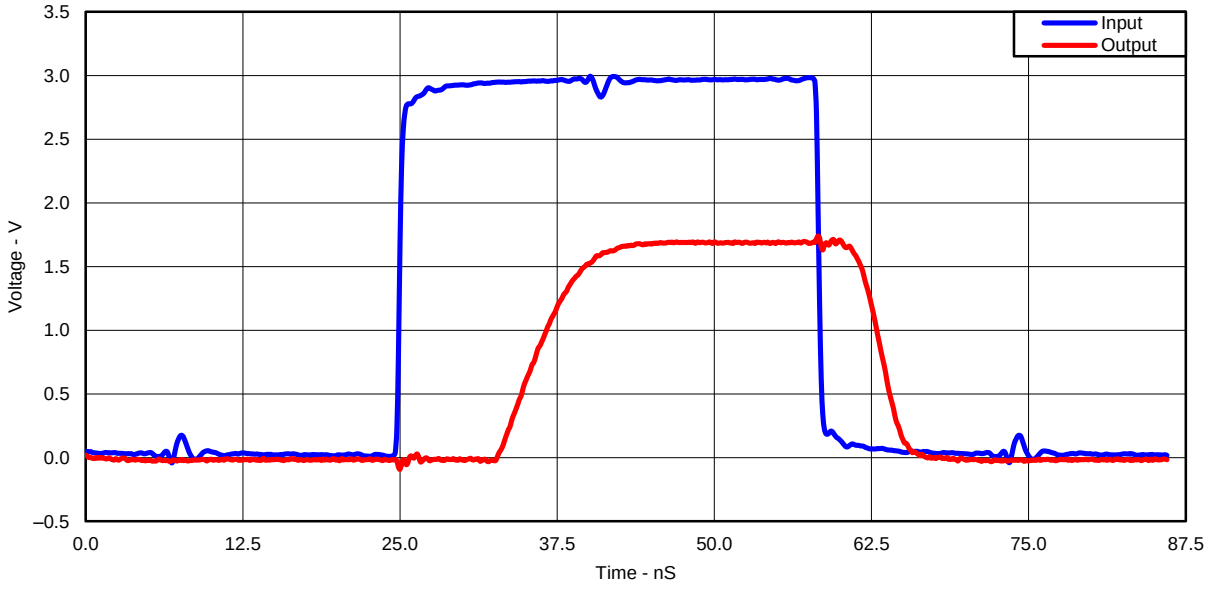


Figure 4. Excellent Signal Integrity (3.3V to 1.8V at 1.8V V_{CC})

4.2 Typical Design Examples

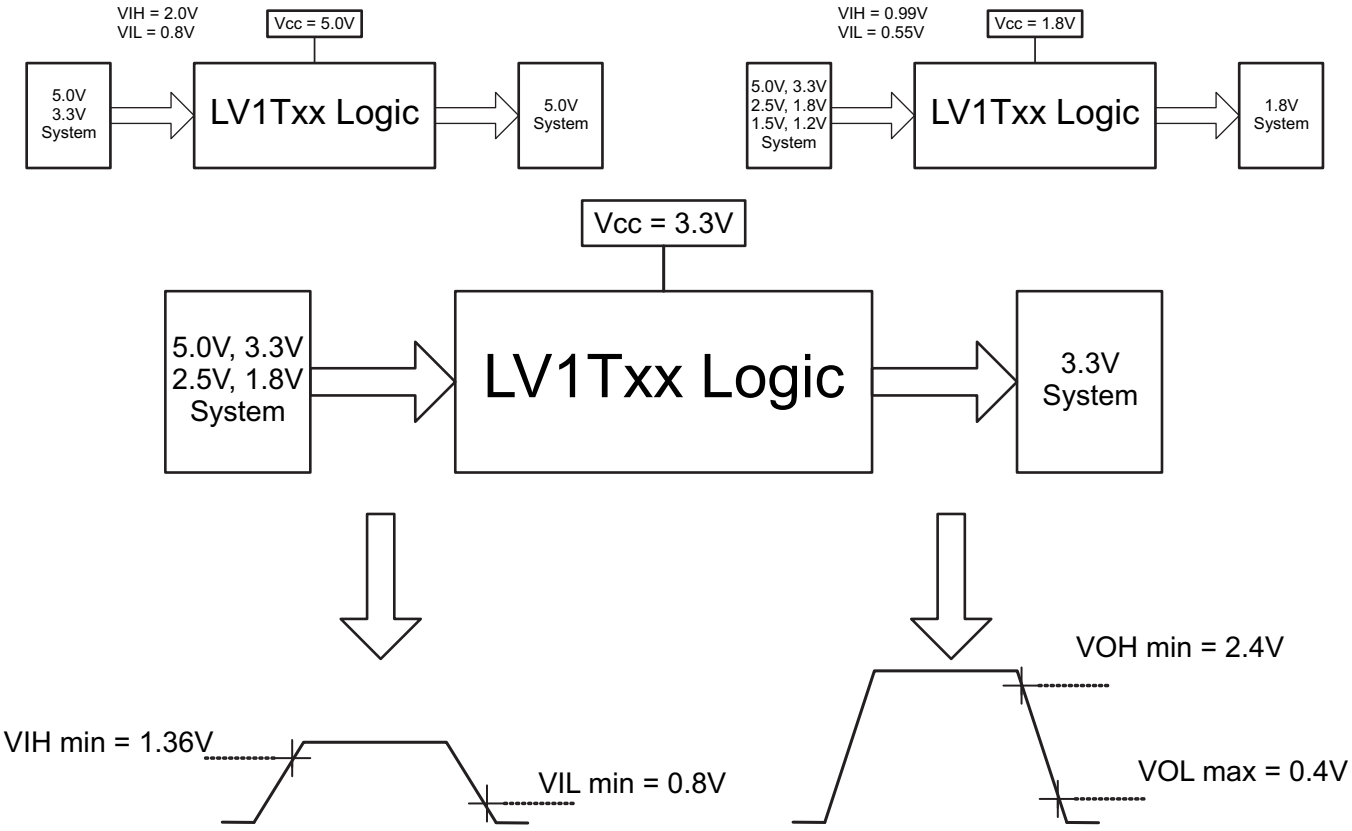


Figure 5. Switching Thresholds for 1.8-V to 3.3-V Translation

4.3 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7.0	V
V_I	Input voltage range(2)		–0.5	7.0	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current			±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DBV package		206	°C/W
		DCK package		252	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

4.4 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		–3.0	mA
		V_{CC} = 2.5 V		–5.0	
		V_{CC} = 3.3 V		–7.0	
		V_{CC} = 5.0 V		–8.0	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		3.0	mA
		V_{CC} = 2.5 V		5.0	
		V_{CC} = 3.3 V		7.0	
		V_{CC} = 5.0 V		8.0	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V		20	ns/V
		V_{CC} = 3.3 V or 2.5 V		20	
		V_{CC} = 5.0 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{IH}	High-level input voltage		V_{CC} = 1.65 V to 1.8 V	0.95			1.0		V
			V_{CC} = 2.0 V	0.99			1.03		
			V_{CC} = 2.25 V to 2.5 V	1.145			1.18		
			V_{CC} = 2.75 V	1.22			1.25		
			$_{VCC}$ = 3.0 V to 3.3 V	1.37			1.39		
			V_{CC} = 3.6 V	1.47			1.48		
			V_{CC} = 4.5 V to 5.0 V	2.02			2.03		
			V_{CC} = 5.5 V	2.1			2.11		
V_{IL}	Low-level input voltage		V_{CC} = 1.65 V to 2.0 V			0.57		0.55	V
			V_{CC} = 2.25 V to 2.75 V			0.75		0.71	
			V_{CC} = 3.0 V to 3.6 V			0.8		0.65	
			V_{CC} = 4.5 V to 5.5 V			0.8		0.8	
V_{OH}		I_{OH} = –20 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –2.0 mA	1.65 V	1.28			1.21		
			1.8 V	1.5			1.45		
		I_{OH} = –3.0 mA	2.3 V	2.0			1.93		
		I_{OH} = –3.0 mA	2.5 V	2.25			2.15		
		I_{OH} = –3.0 mA	3.0 V	2.78			2.7		V
		I_{OH} = –5.5 mA		2.6			2.49		
		I_{OH} = –5.5 mA	3.3 V	2.9			2.8		
		I_{OH} = –4.0 mA	4.5 V	4.2			4.1		
		I_{OH} = –8.0 mA		4.1			3.95		
		I_{OH} = –8.0 mA	5.0 V	4.6			4.5		
V_{OL}		I_{OL} = 20 µA	1.65 V to 5.5 V			0.1		0.1	V
		I_{OL} = 2.0 mA	1.65 V			0.2		0.25	
		I_{OH} = 3.0 mA	2.3 V			0.15		0.2	
		I_{OL} = 3.0 mA	3.0 V			0.11		0.15	
		I_{OL} = 5.5 mA				0.21		0.252	
		I_{OL} = 4.0 mA	4.5 V			0.15		0.2	
		I_{OL} = 8.0 mA				0.3		0.35	
I_I	A input	V_I = 0 V or V_{CC}	0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V			0.1		±1.0	µA
I_{CC}		V_I = 0 V or V_{CC}; I_O = 0; Open on loading	5.0 V			1.0		10.0	µA
			3.3 V			1.0		10.0	
			2.5 V			1.0		10.0	
			1.8 V			1.0		10.0	
ΔI_{CC}		One input at 0.3 V or 3.4 V Other inputs at 0 or V_{CC}, I_O = 0	5.5 V			1.35		1.5	mA
		One input at 0.3 V or 1.1 V Other inputs at 0 or V_{CC}, I_O = 0	1.8 V			10.0		10.0	µA
C_i		V_I = V_{CC} or GND	3.3 V		2.0	10.0	2.0	10.0	pF
C_o		V_O = V_{CC} or GND	3.3 V		2.5		2.5		pF

4.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

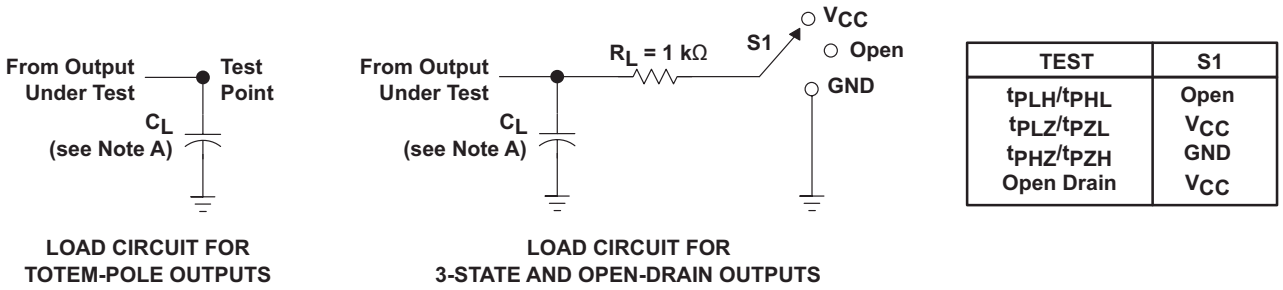
PARAMETER	FROM (INPUT)	TO (OUTPUT)	FREQUENCY (TYP)	V_{CC}	C_L	T_A = 25°C			T_A = –65°C to 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Any In	Y	DC to 50 MHz	5.0 V	15 pF		2.7	5.5		3.4	6.5	ns
					30 pF		3.0	6.5		4.1	7.5	
				3.3 V	15 pF		4.0	7.0		5.0	8.0	ns
					30 pF		4.9	8.0		6.0	9.0	
			DC to 25 MHz	2.5 V	15 pF		5.8	8.5		6.8	9.5	ns
					30 pF		6.5	9.5		7.5	10.5	
			DC to 15 MHz	1.8 V	15 pF		10.5	13.0		11.8	14.0	ns
					30 pF		12.0	14.5		12.0	15.5	
t_{PZH}, t_{PZL}	OE	Y	DC to 50 MHz	5.0 V	15 pF		3.0	5.0		3.5	6.0	ns
					30 pF		4.3	6.5		4.9	7.5	
				3.3 V	15 pF		4.0	6.5		4.5	7.5	ns
					30 pF		5.0	8.0		6.5	9.0	
			DC to 25 MHz	2.5 V	15 pF		5.5	8.0		6.1	9.0	ns
					30 pF		7.0	10.0		8.5	11.0	
			DC to 15 MHz	1.8 V	15 pF		9.0	12.0		9.85	13.0	ns
					30 pF		12.5	15.0		13.5	16.0	
t_{PHZ}, t_{PLZ}	OE	Y	DC to 50 MHz	5.0 V	15 pF		4.2	6.5		4.5	7.0	ns
					30 pF		4.8	8.0		5.0	8.5	
				3.3 V	15 pF		4.5	7.0		5.0	8.0	ns
					30 pF		5.0	8.0		5.5	9.0	
			DC to 25 MHz	2.5 V	15 pF		5.0	11.0		6.0	9.0	ns
					30 pF		6.0	9.0		7.0	10.0	
			DC to 15 MHz	1.8 V	15 pF		8.0	10.0		8.5	11.0	ns
					30 pF		8.5	11.0		9.5	12.0	

4.7 Operating Characteristics

over operating free-air temperature range (unless otherwise noted)

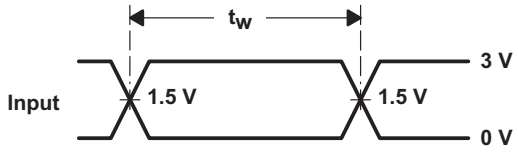
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 1 MHz and 10 MHz	1.8 V ± 0.15 V	14	pF
			2.5 V ± 0.2 V	14	
			3.3 V ± 0.3 V	14	
			5.0 V ± 0.5 V	14	

5 Parameter Measurement Information

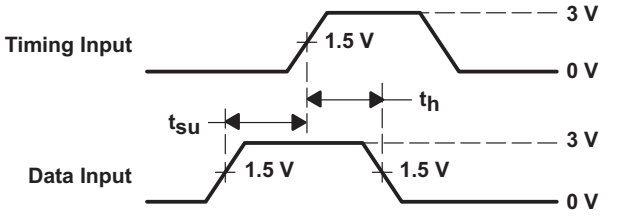


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

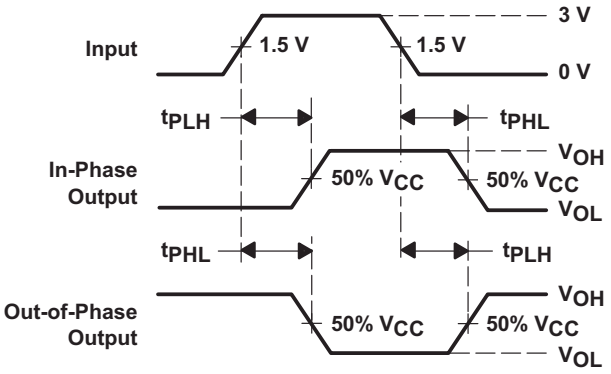
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



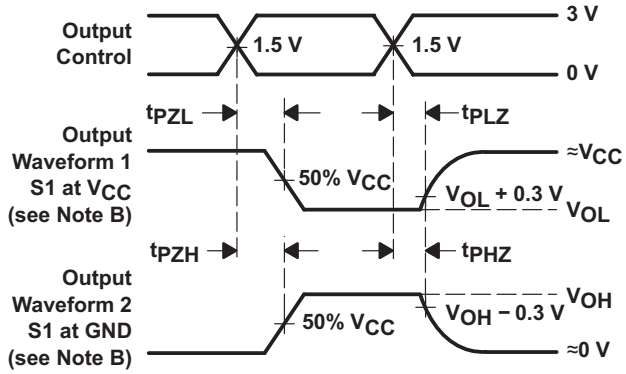
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 6. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

5.1 More Product Selection

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T125	DCK, DBV, DPW	Single Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV1T125	DCK, DBV	Single Buffer Gate with 3-state Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

6 Device and Documentation Support

6.1 Trademarks

All trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

7 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV1T125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(NEZ3 ~ NEZS)	Samples
SN74LV1T125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(WZ3 ~ WZS)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

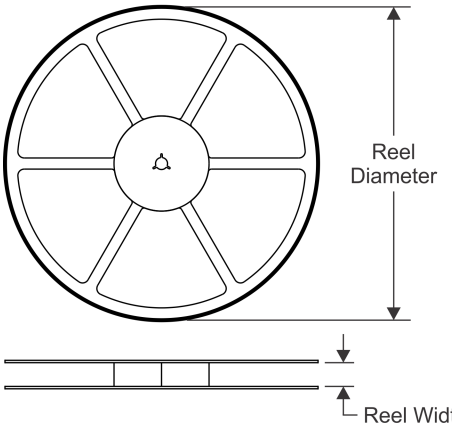
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

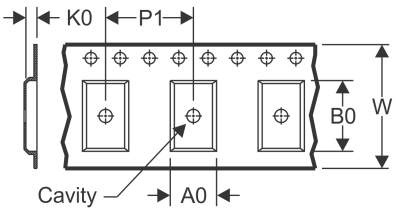
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

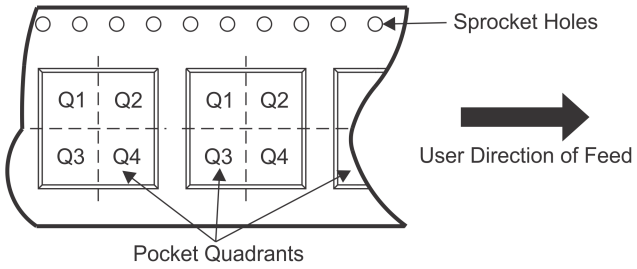


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

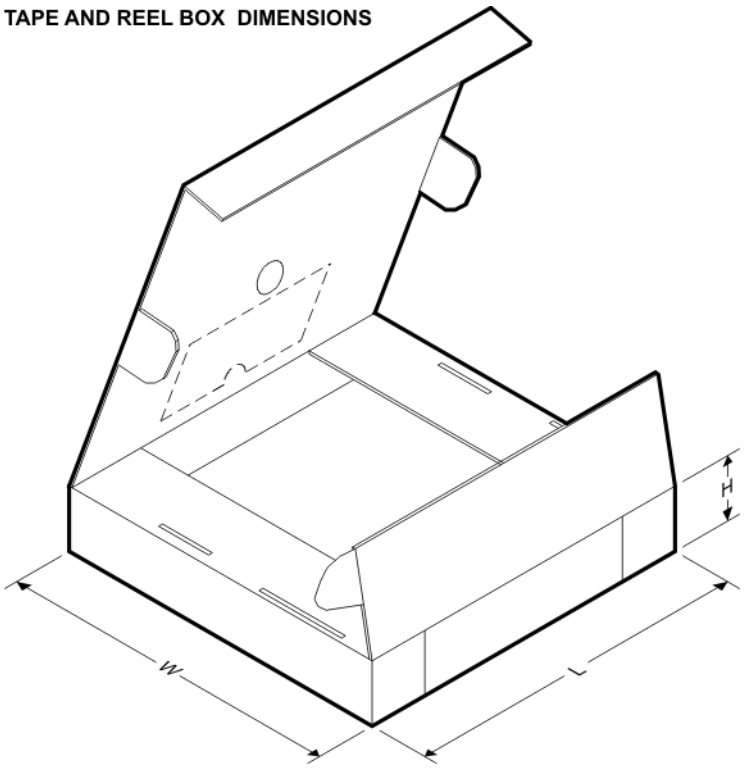
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LV1T125DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LV1T125DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LV1T125DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

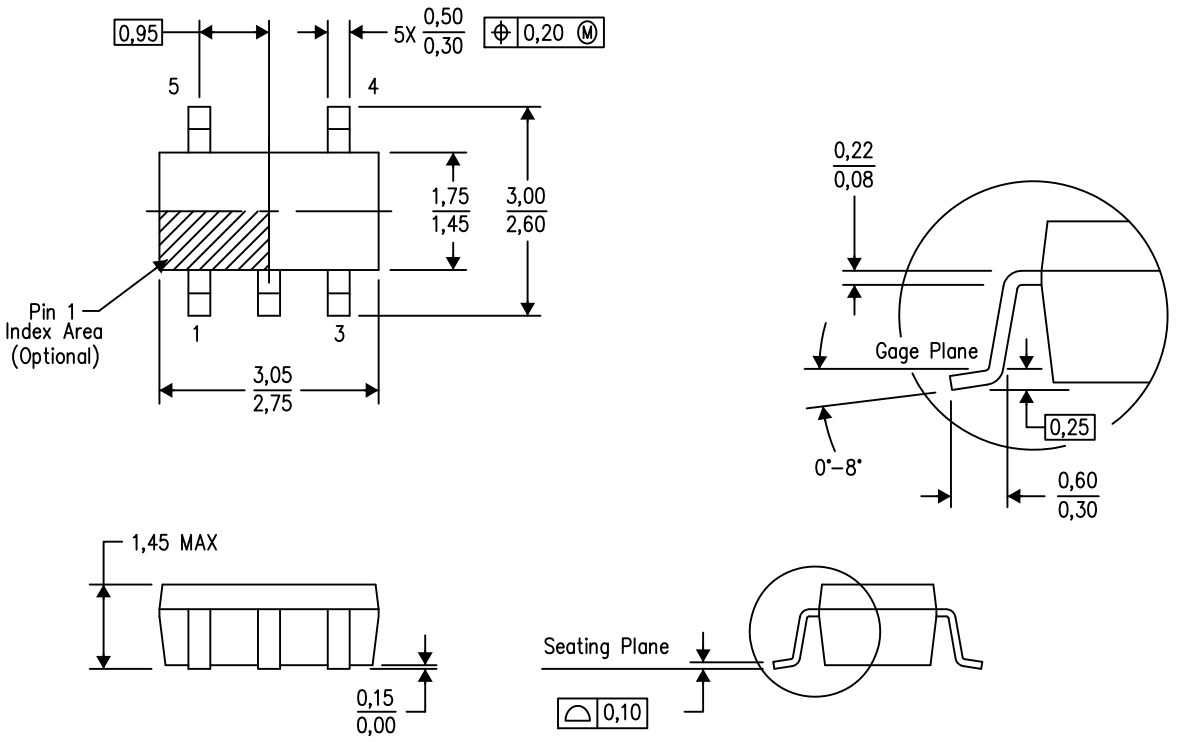
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LV1T125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T125DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LV1T125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

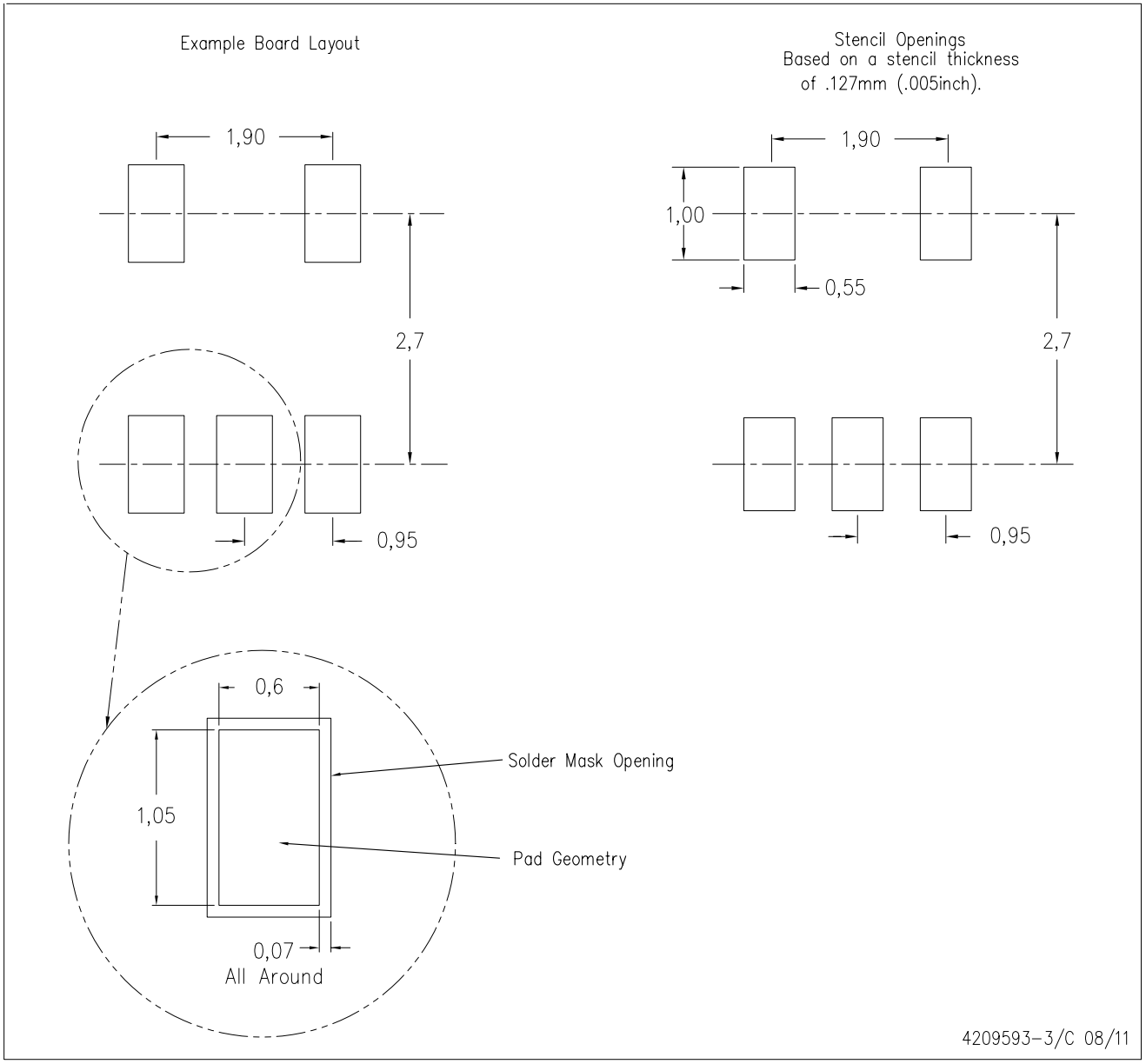
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

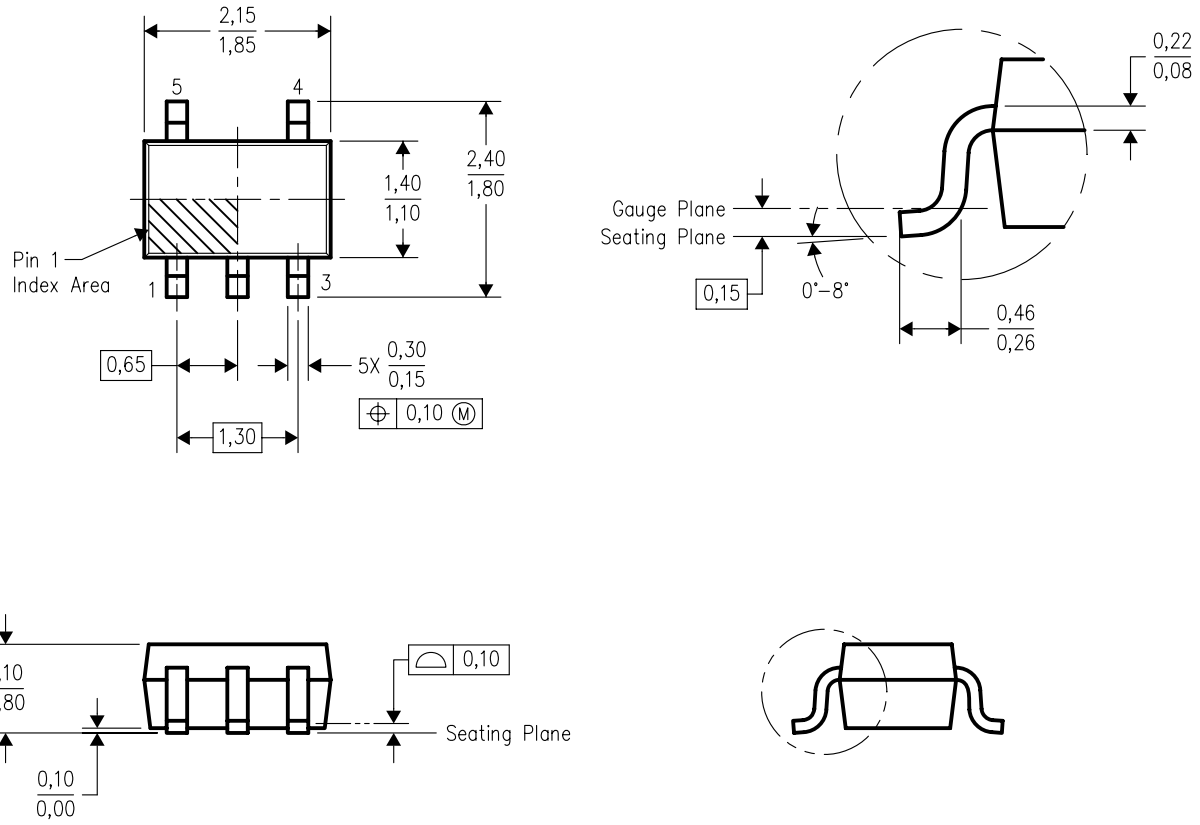
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

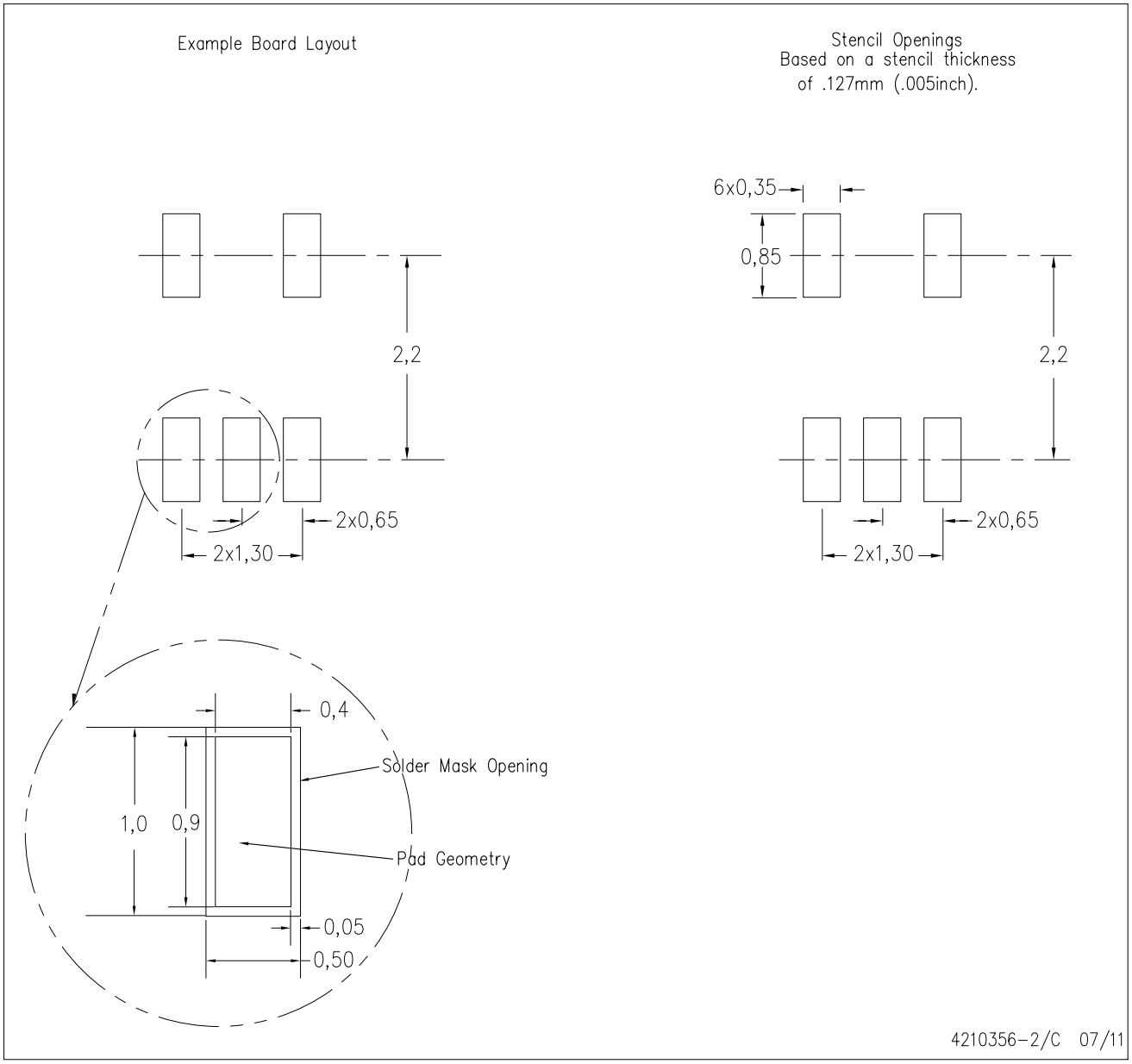
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
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